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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/717,570	11/21/2003	Kunihiko Yahagi	245824US2	8449

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EXAMINER	
MCLEAN MAYO, KIMBERLY N	
ART UNIT	**PAPER NUMBER**
2187	

DATE MAILED: 02/28/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/717,570	YAHAGI, KUNIHIKO	
	Examiner	Art Unit	
	Kimberly N. McLean-Mayo	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 18-20* is/are rejected.

7)☒ Claim(s) *2-17* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2/18/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The enclosed detailed action is in response to the Information Disclosure Statement, Priority Papers and the Application submitted on November 21, 2003.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Andrewartha (USPN: 5,754,557) in view of van der Wal et al. (USPN: 6,151,682).

Regarding claims 1 and 20, Andrewartha discloses a state generator (comprised of the state machines) configured to generate a plurality of state information signals in response to command requests associated with a plurality of banks in a memory (C 3, L 10-12); a bank controller configured to generate a command based on the state information signals (C 3, L 7-12). Andrewartha does disclose an enable signal generator configured to generate a plurality of enable signals indicating whether the state information signals are valid or not. However, van der Wal teaches the concept of generating enable signals (timing signals) to indicate whether the an output signal(s) is valid or not (C 4, L 51-53). van der Wal provides this feature to resolve timing issues inherent in digital designs implemented in ASICs, FPGAs (C 1, L 50 +). Andrewartha's state machine is implemented in ASIC and thus is susceptible to the same timing issues (C 3, L 5-6). Hence, it would have been obvious to one of ordinary skill in the art to

incorporate the teachings of van der Wal in the system taught by Andrewartha such that the bank controller would generate a command based on the state information signals and the enable signals for the desirable purpose of resolving any timing issues with respect to the state signals thereby providing accuracy.

4. Claims 18-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Andrewartha (USPN: 5,754,557) in view of van der Wal et al. (USPN: 6,151,682) and Valmiki (USPN: 6,661,422).

Regarding claims 18-19, Andrewartha discloses memory controller comprising a state generator (comprised of the state machines) configured to generate a plurality of state information signals in response to command requests associated with a plurality of banks in a memory (C 3, L 10-12); a bank controller configured to generate a command based on the state information signals (C 3, L 7-12). Andrewartha does disclose an enable signal generator configured to generate a plurality of enable signals indicating whether the state information signals are valid or not. However, van der Wal teaches the concept of generating enable signals (timing signals) to indicate whether the an output signal(s) is valid or not (C 4, L 51-53). van der Wal provides this feature to resolve timing issues inherent in digital designs implemented in ASICs, FPGAs (C 1, L 50 +). Andrewartha's state machine is implemented in ASIC and thus is susceptible to the same timing issues (C 3, L 5-6). Hence, it would have been obvious to one of ordinary skill in the art to incorporate the teachings of van der Wal in the system taught by Andrewartha such that the bank controller would generate a command based on the state information signals and the enable signals for the desirable purpose of resolving any timing issues with respect to the state

signals thereby providing accuracy. Additionally, Andrewartha and van der Wal do not disclose the memory controller integrated on semiconductor chip with a signal processor configured to perform signal processing and to transmit command requests to the memory controller. Although, the signal processor is not explicitly disclosed, it is evident that such logic exists and that the memory device is intended to be used with other logic. Memory devices are not stand-alone devices. However, Valmiki discloses a processor integrated on a semiconductor chip with a memory controller (C 128, L 20 +). This feature provides space efficiency and improves speed of data transfers by reducing the delays associated with external (off-chip) interfaces. Hence, it would have been obvious to one of ordinary skill in the art to the above features taught by Andrewartha and van der Wal on an integrated chip with a signal processor for the desirable purpose of practicality, space efficiency and reduced delays.

Allowable Subject Matter

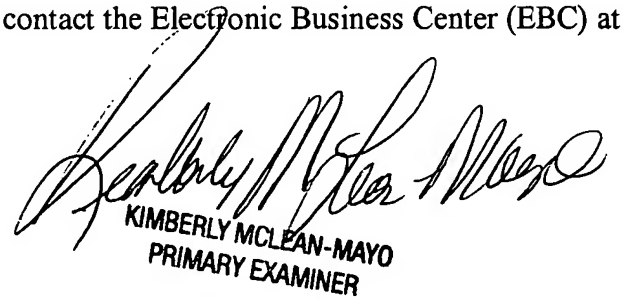
5. Claims 2-17 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kimberly N. McLean-Mayo whose telephone number is 571-272-4194. The examiner can normally be reached on Mon, Wed, Thurs. (10-4), Tues, (9:45- 6:15) .

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks can be reached on 571-272-4201. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Kimberly N. McLean-Mayo
Primary Examiner
Art Unit 2187

KNM

February 18, 2006